FIG. 1

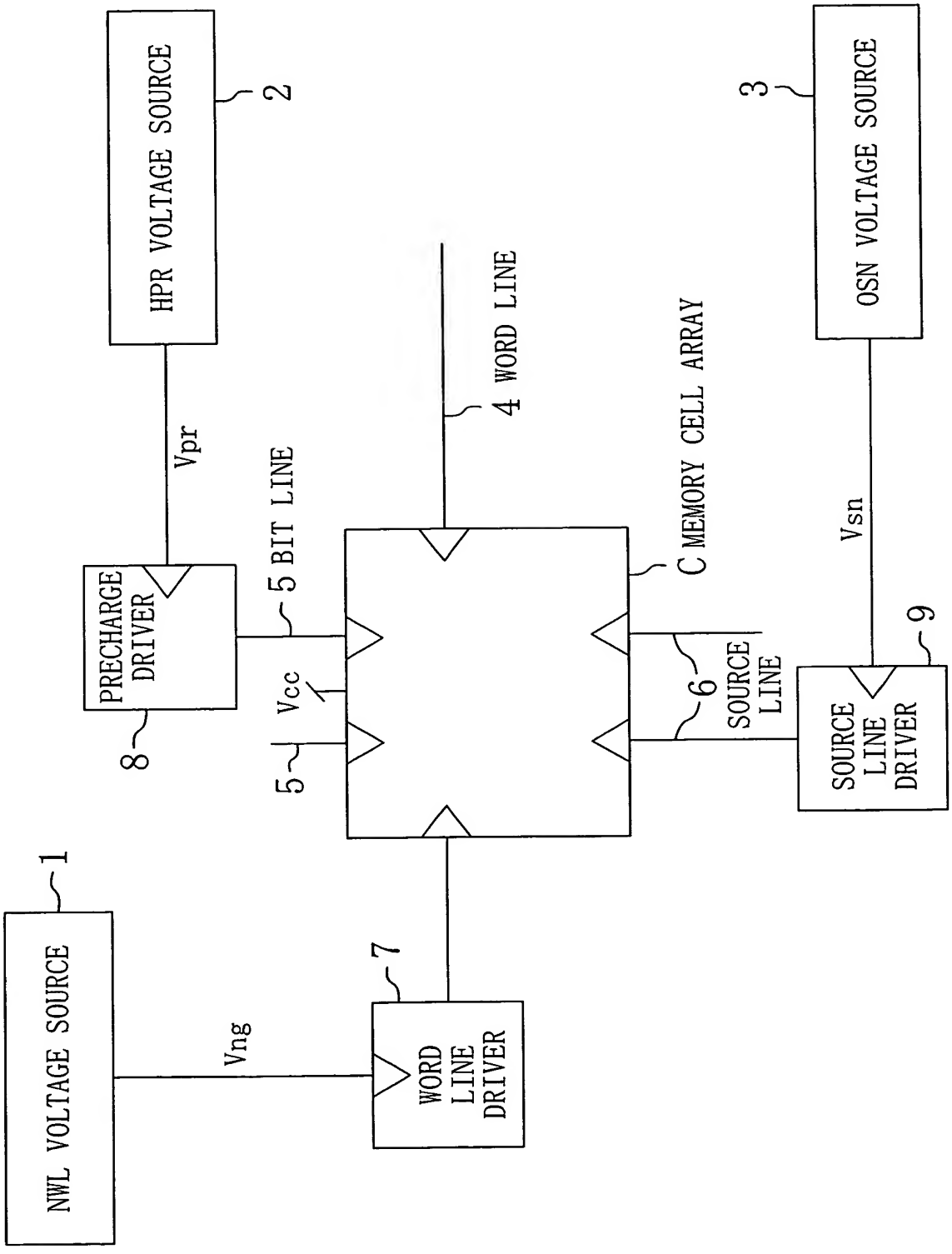

HPR VOLTAGE SOURCE
2
OSN VOLTAGE SOURCE
3
Vpr
4 WORD LINE
5 BIT LINE
C MEMORY CELL ARRAY
Vsn
PRECHARGE DRIVER
8
Vcc
1
5
6
SOURCE LINE
SOURCE LINE DRIVER
9
NWL VOLTAGE SOURCE
1
Vng
7
WORD LINE DRIVER

FIG. 2

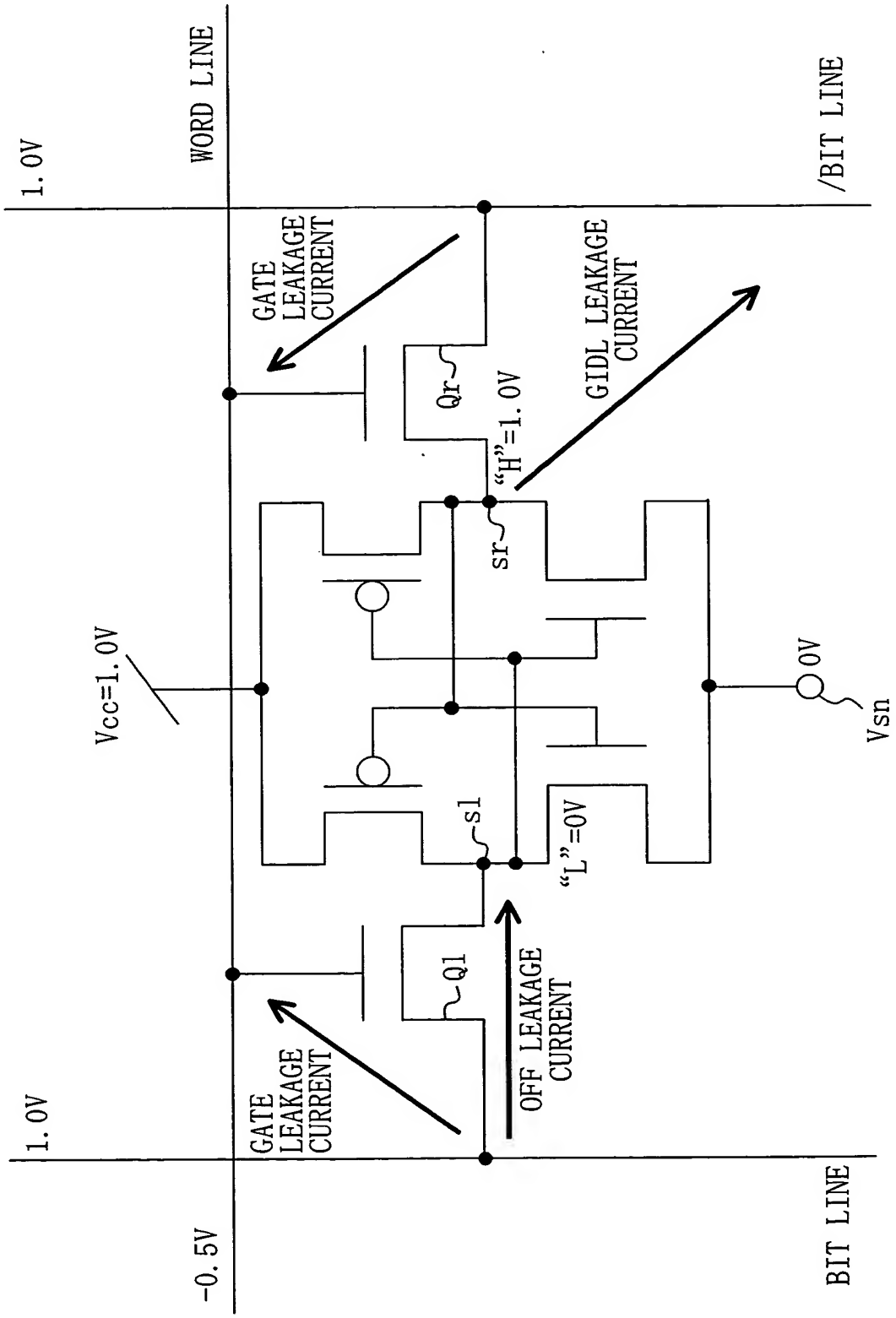

1.0V
WORD LINE
/BIT LINE
GATE LEAKAGE CURRENT
Qr
"H"=1.0V
GIDL LEAKAGE CURRENT
sr
Vcc=1.0V
0V
Vsn
sl
"L"=0V
Q1
OFF LEAKAGE CURRENT
GATE LEAKAGE CURRENT
1.0V
-0.5V
BIT LINE

FIG. 3

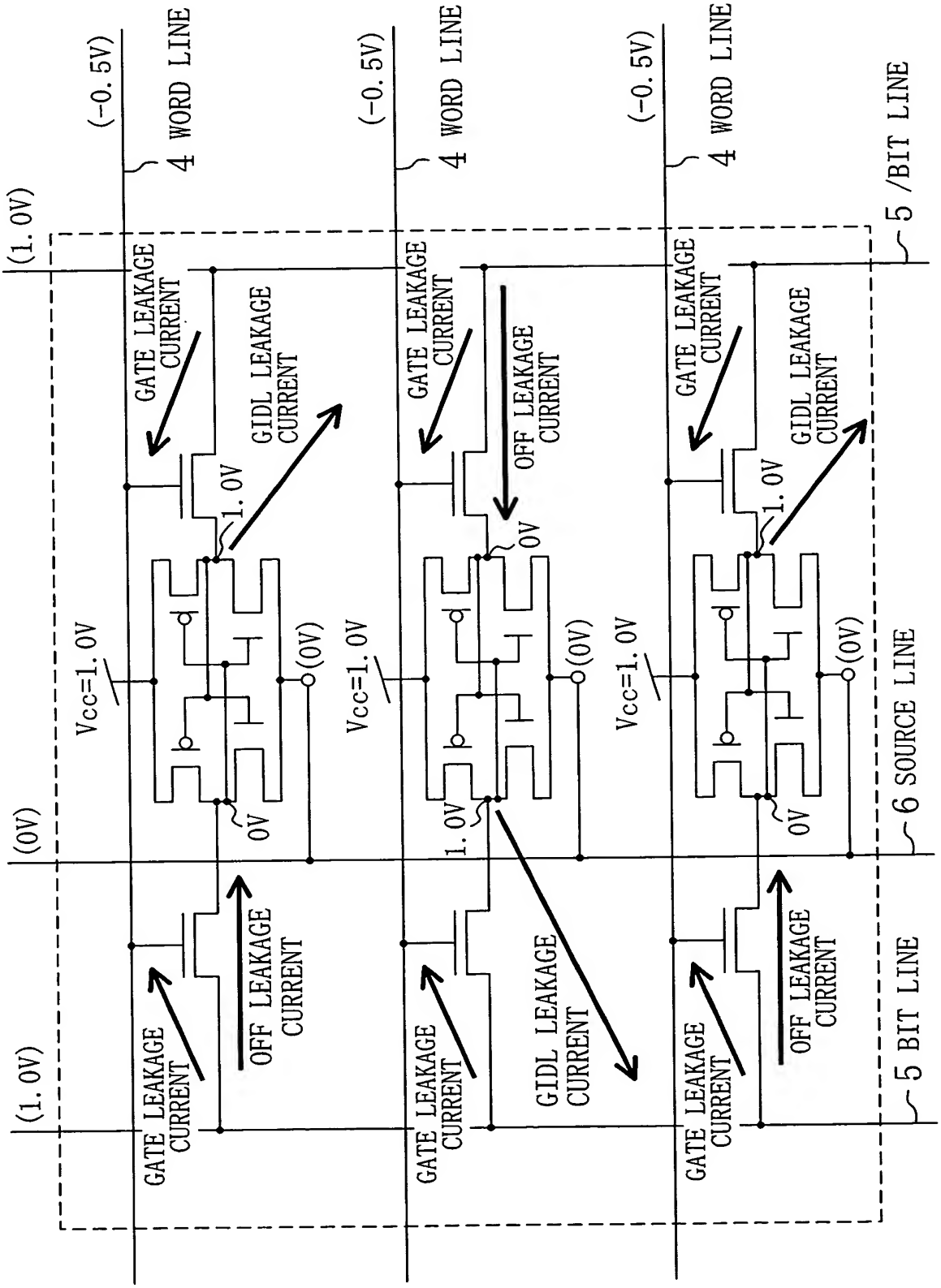

(-0.5V)
4 WORD LINE
(1.0V)
5 /BIT LINE
GATE LEAKAGE CURRENT
GIDL LEAKAGE CURRENT
OFF LEAKAGE CURRENT
Vcc=1.0V
1.0V
0V
(0V)
6 SOURCE LINE
5 BIT LINE

FIG. 4

NON-SELECTED WORD LINE (NWL VOLTAGE SOURCE)		LARGE NEGATIVE VOLTAGE (-Vcc～-Vcc/2)	INTERMEDIATE NEGATIVE VOLTAGE (-Vcc/3～-Vcc/4)	SMALL NEGATIVE VOLTAGE (-Vcc/6～0V)
	OFF LEAKAGE CURRENT	VERY SMALL	INTERMEDIATE	VERY LARGE
	GATE LEAKAGE CURRENT	VERY LARGE	INTERMEDIATE	SMALL
	GIDL LEAKAGE CURRENT	VERY LARGE	INTERMEDIATE	SMALL
NON-SELECTED BIT LINE (HPR VOLTAGE SOURCE)		HIGH POTENTIAL PRECHARGE (Vpre=Vcc)	INTERMEDIATE POTENTIAL PRECHARGE (Vpre=Vcc/2)	LOW POTENTIAL PRECHARGE (Vpre=Vcc/3～0V)
	OFF LEAKAGE CURRENT	INTERMEDIATE	SMALL	INTERMEDIATE
	GATE LEAKAGE CURRENT	LARGE	SMALL	LARGE
	GIDL LEAKAGE CURRENT	LARGE	SMALL	LARGE
NON-SELECTED SOURCE LINE (OSN VOLTAGE SOURCE)		HIGH POTENTIAL LOW LEVEL (Vsn=Vcc/2)	INTERMEDIATE POTENTIAL LOW LEVEL (Vsn=Vcc/4)	LOW POTENTIAL LOW LEVEL (Vsn=0V)
	OFF LEAKAGE CURRENT	VERY SMALL (DATA RETENTION UNSTABLE)	INTERMEDIATE	LARGE
	GATE LEAKAGE CURRENT	UNRELATED (DATA RETENTION UNSTABLE)	UNRELATED	UNRELATED
	GIDL LEAKAGE CURRENT	VERY SMALL (DATA RETENTION UNSTABLE)	INTERMEDIATE	SMALL

FIG. 5

	STATE	VOLTAGE SOURCE	SELECTED	NON-SELECTED
DURING OPERATION	Mode-A (HIGH TEMPERATURE)	NWL VOLTAGE SOURCE (WORD LINE)	Vcc	-1/3 Vcc
		HPR VOLTAGE SOURCE (BIT LINE)	1/2 Vcc~Vcc	1/2 Vcc
		OSN VOLTAGE SOURCE (SOURCE LINE)	Vss	1/3 Vcc
	Mode-B (LOW TO ROOM TEMPERATURE)	NWL VOLTAGE SOURCE (WORD LINE)	Vcc	-1/4 Vcc
		HPR VOLTAGE SOURCE (BIT LINE)	1/2 Vcc~Vcc	1/2 Vcc
		OSN VOLTAGE SOURCE (SOURCE LINE)	Vss	1/4 Vcc
DURING STANDBY	Mode-C (HIGH TEMPERATURE)	NWL VOLTAGE SOURCE (WORD LINE)		-1/3 Vcc
		HPR VOLTAGE SOURCE (BIT LINE)		floating
		OSN VOLTAGE SOURCE (SOURCE LINE)		1/3 Vcc
	Mode-D (LOW TO ROOM TEMPERATURE)	NWL VOLTAGE SOURCE (WORD LINE)		-1/4 Vcc
		HPR VOLTAGE SOURCE (BIT LINE)		floating
		OSN VOLTAGE SOURCE (SOURCE LINE)		1/4 Vcc

FIG. 6

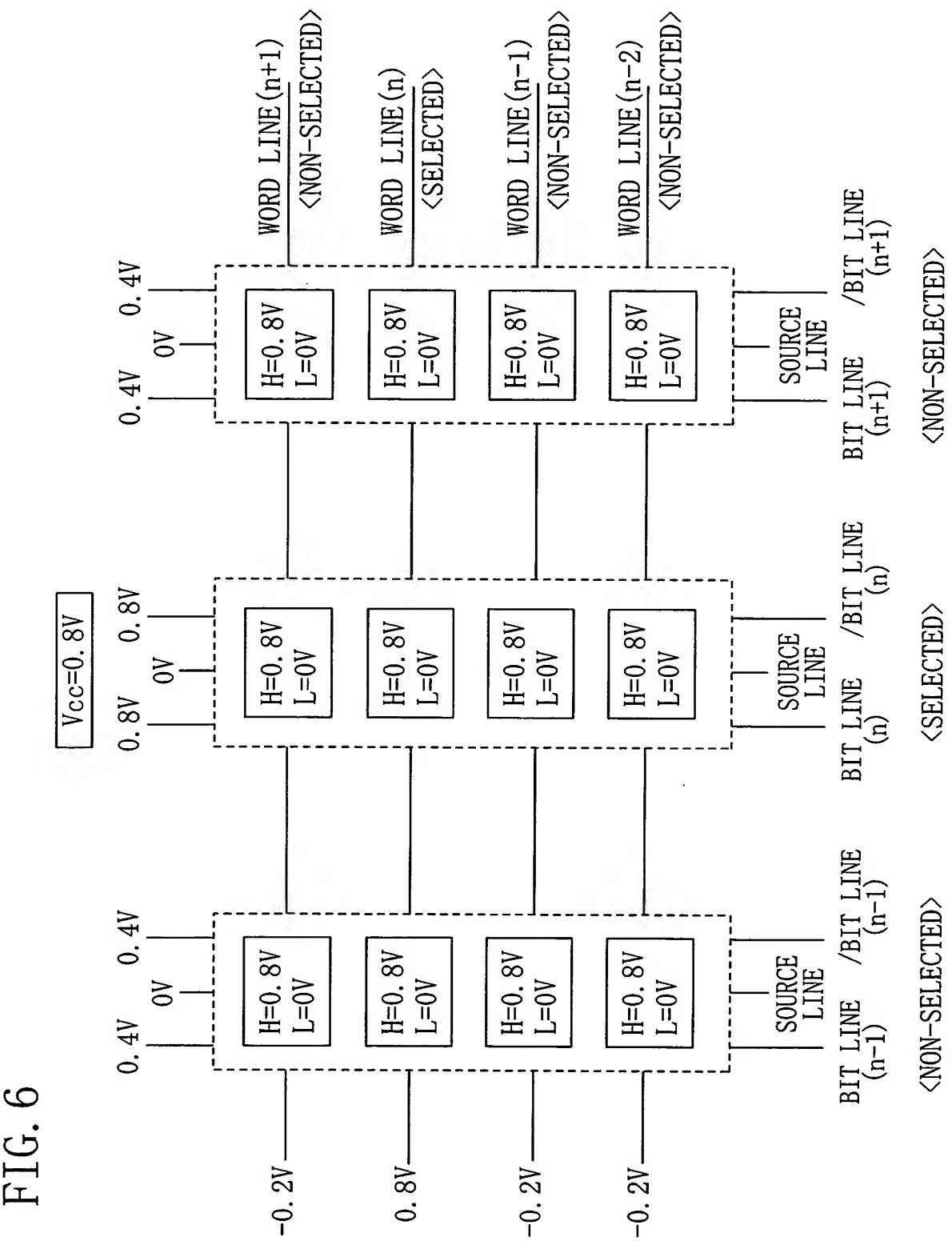

Vcc=0.8V
WORD LINE(n+1)
<NON-SELECTED>
WORD LINE(n)
<SELECTED>
WORD LINE(n-1)
<NON-SELECTED>
WORD LINE(n-2)
<NON-SELECTED>
0.4V
0V
0.4V
0.8V
0V
0.8V
H=0.8V
L=0V
SOURCE LINE
BIT LINE (n-1)
/BIT LINE (n-1)
BIT LINE (n)
/BIT LINE (n)
BIT LINE (n+1)
/BIT LINE (n+1)
<NON-SELECTED>
<SELECTED>
<NON-SELECTED>
-0.2V
0.8V
-0.2V
-0.2V

FIG. 7

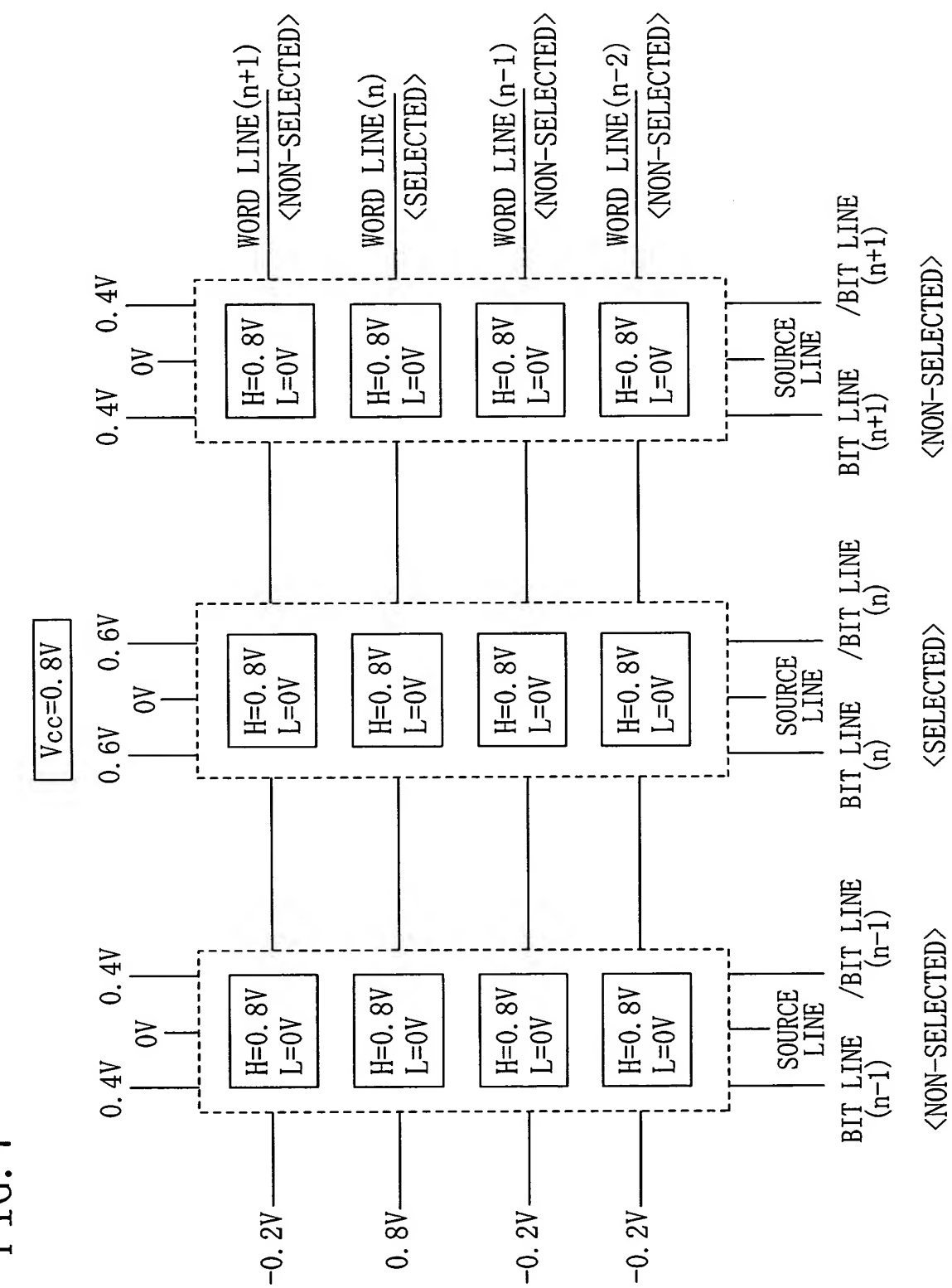

Vcc=0.8V
WORD LINE(n+1)
<NON-SELECTED>
WORD LINE(n)
<SELECTED>
WORD LINE(n-1)
<NON-SELECTED>
WORD LINE(n-2)
<NON-SELECTED>
0.4V
0V
0.4V
0.6V
0V
0.6V
0.4V
0V
0.4V
H=0.8V
L=0V
SOURCE LINE
-0.2V
0.8V
-0.2V
-0.2V
BIT LINE (n-1)
/BIT LINE (n-1)
BIT LINE (n)
/BIT LINE (n)
BIT LINE (n+1)
/BIT LINE (n+1)
<NON-SELECTED>
<SELECTED>
<NON-SELECTED>

FIG. 8

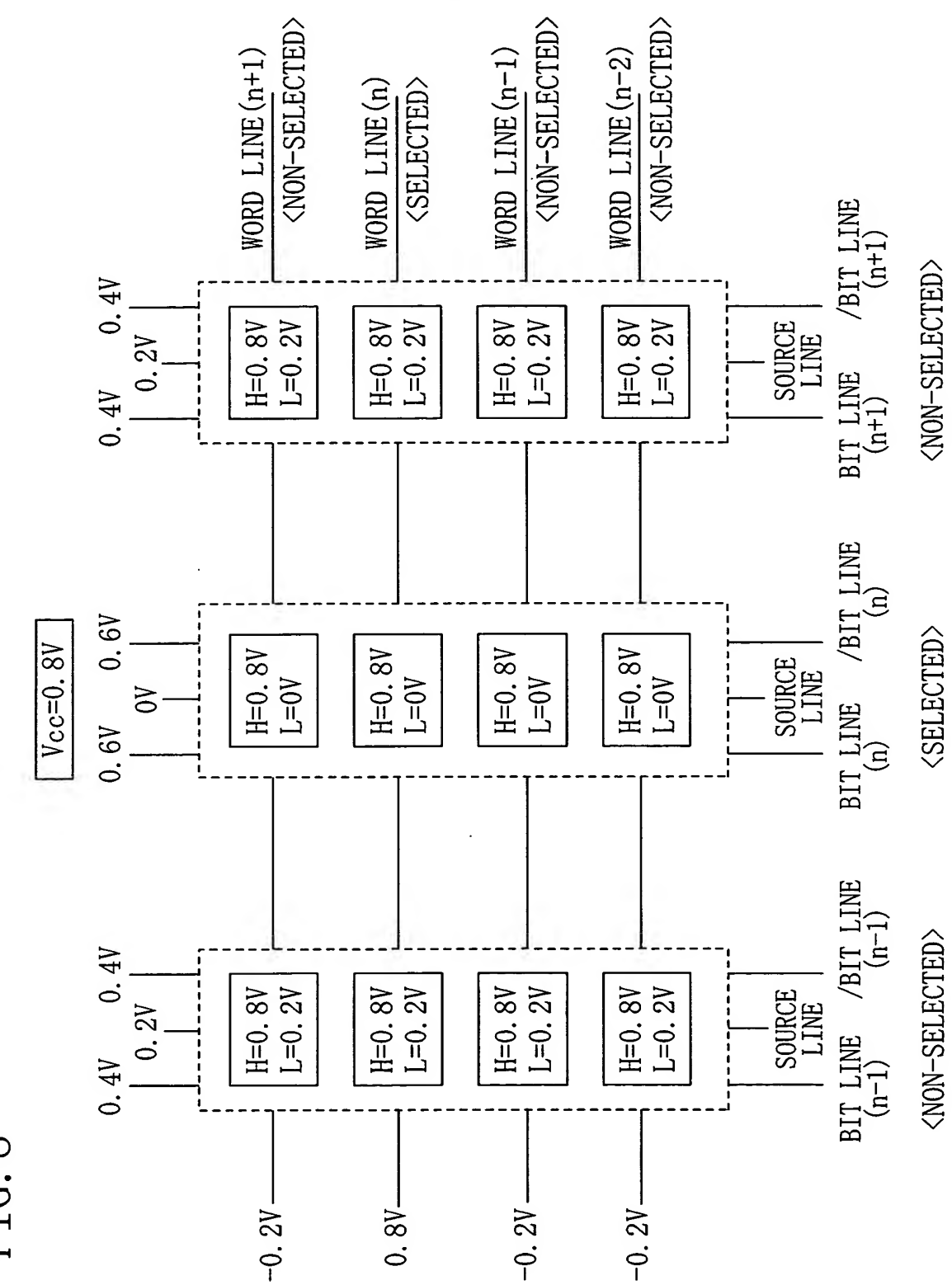

Vcc=0.8V
WORD LINE(n+1)
<NON-SELECTED>
WORD LINE(n)
<SELECTED>
WORD LINE(n-1)
<NON-SELECTED>
WORD LINE(n-2)
<NON-SELECTED>
0.4V
0.2V
0.4V
0.4V
0.6V
0V
0.6V
0.4V
0.2V
0.4V
H=0.8V
L=0.2V
H=0.8V
L=0V
SOURCE LINE
BIT LINE (n-1)
/BIT LINE (n-1)
BIT LINE (n)
/BIT LINE (n)
BIT LINE (n+1)
/BIT LINE (n+1)
-0.2V
0.8V
-0.2V
-0.2V
<NON-SELECTED>
<SELECTED>
<NON-SELECTED>

FIG. 9

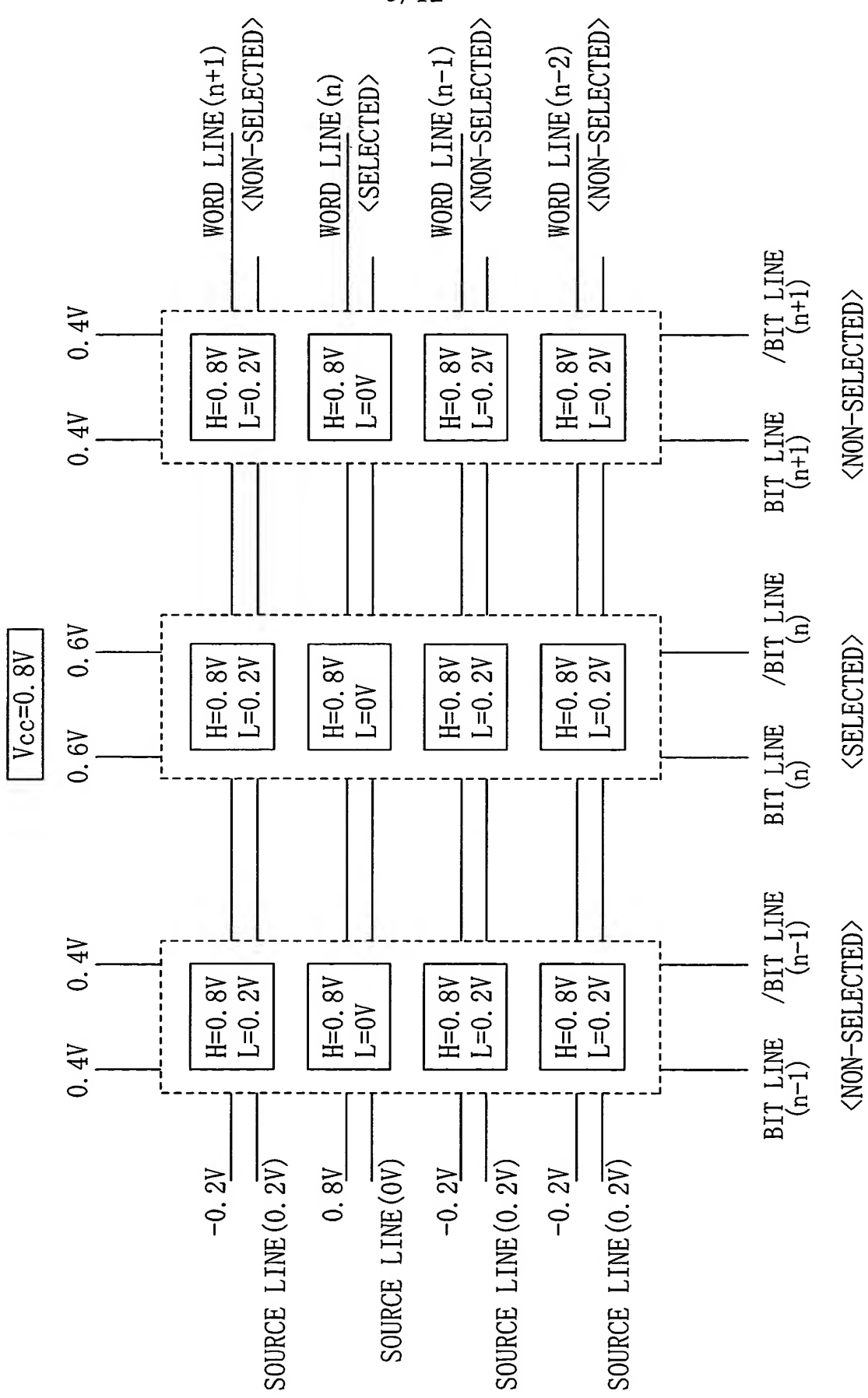

Vcc=0.8V
WORD LINE(n+1)
<NON-SELECTED>
WORD LINE(n)
<SELECTED>
WORD LINE(n-1)
<NON-SELECTED>
WORD LINE(n-2)
<NON-SELECTED>
0.4V
0.4V
0.6V
0.6V
0.4V
0.4V
H=0.8V
L=0.2V
H=0.8V
L=0V
-0.2V
0.8V
-0.2V
-0.2V
SOURCE LINE(0.2V)
SOURCE LINE(0V)
SOURCE LINE(0.2V)
SOURCE LINE(0.2V)
BIT LINE (n-1)
/BIT LINE (n-1)
BIT LINE (n)
/BIT LINE (n)
BIT LINE (n+1)
/BIT LINE (n+1)
<NON-SELECTED>
<SELECTED>
<NON-SELECTED>

FIG. 10

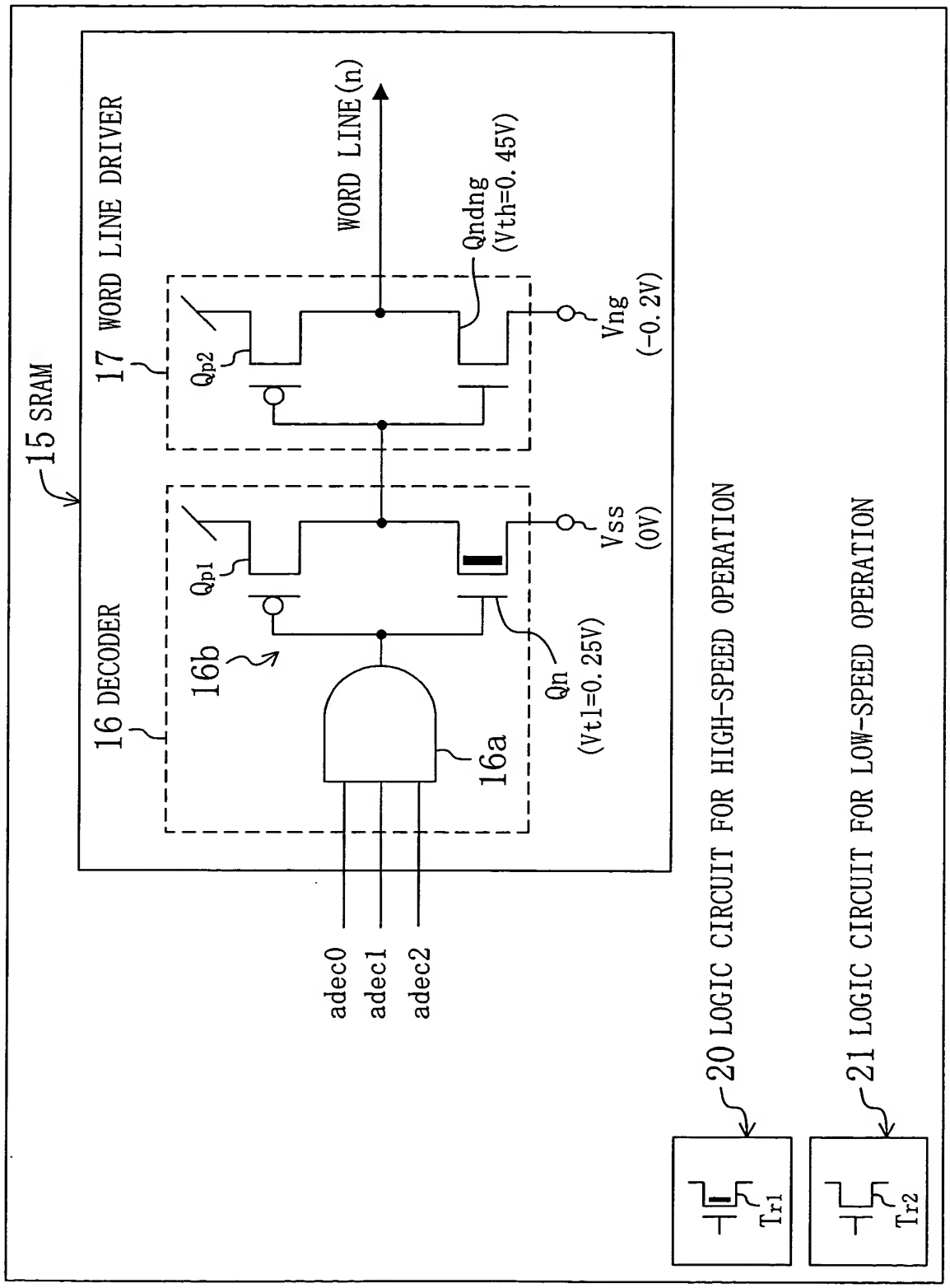

15 SRAM
16 DECODER
16a
16b
17 WORD LINE DRIVER
Qp1
Qp2
Qn
(Vt1=0.25V)
Qndng
(Vth=0.45V)
WORD LINE(n)
Vss
(0V)
Vng
(-0.2V)
adec0
adec1
adec2
20 LOGIC CIRCUIT FOR HIGH-SPEED OPERATION
21 LOGIC CIRCUIT FOR LOW-SPEED OPERATION
Tr1
Tr2

FIG. 11

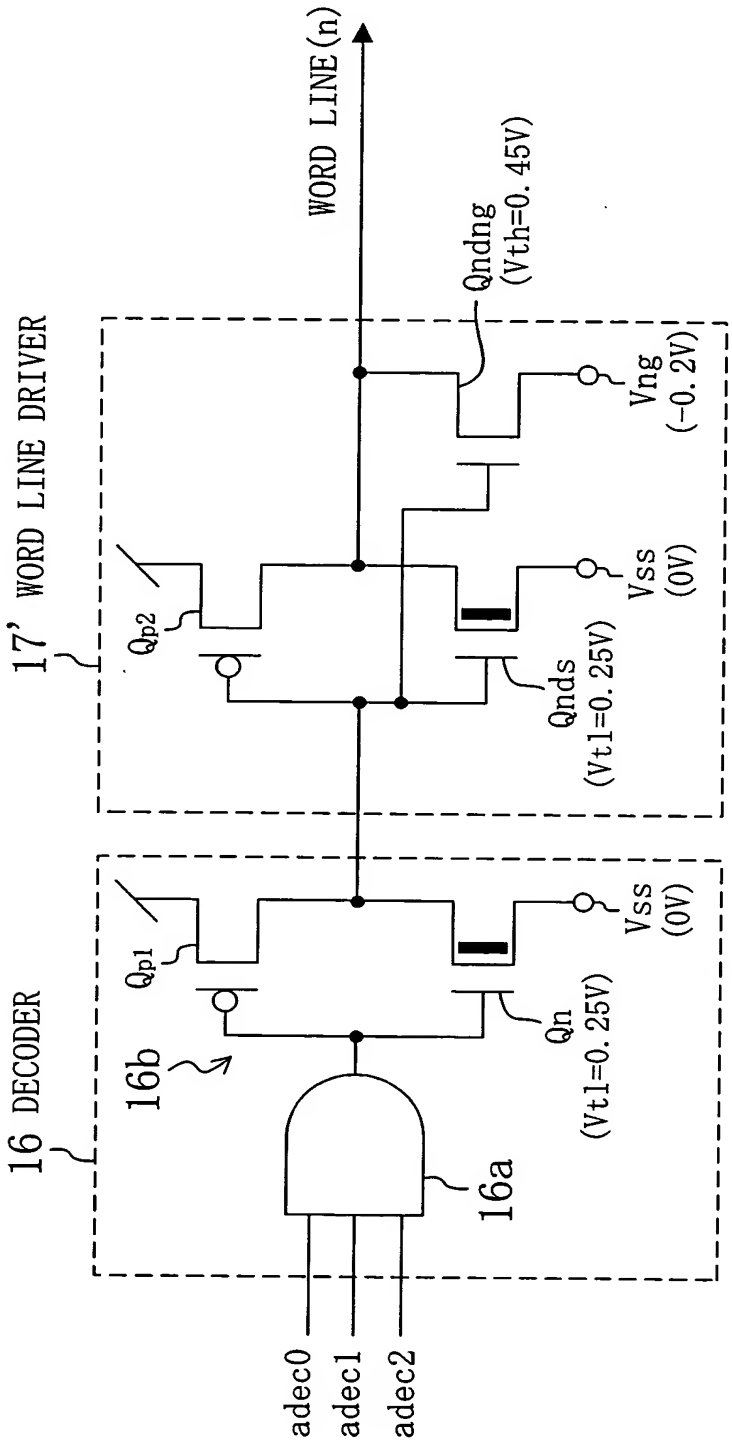
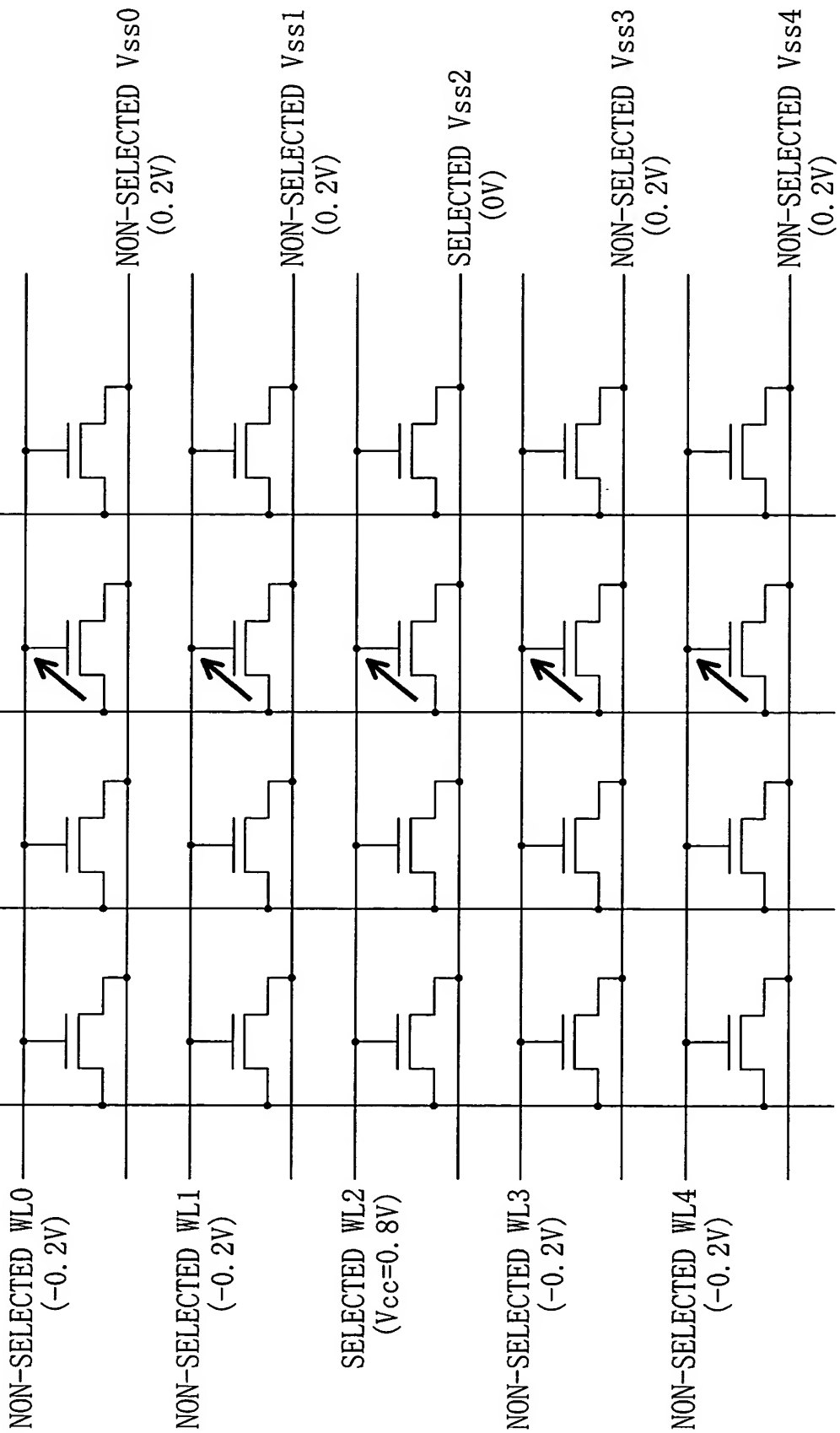

WORD LINE(n)
17' WORD LINE DRIVER
16 DECODER
Qndng
(Vth=0.45V)
Vng
(-0.2V)
Qp2
Vss
(0V)
Qnds
(Vtl=0.25V)
Qp1
Vss
(0V)
16b
Qn
(Vtl=0.25V)
16a
adec0
adec1
adec2

FIG. 12


NON-SELECTED BL0 (0V)
NON-SELECTED BL1 (0V)
SELECTED BL2 (0.6V)
NON-SELECTED BL3 (0V)
NON-SELECTED WL0 (-0.2V)
NON-SELECTED WL1 (-0.2V)
SELECTED WL2 (Vcc=0.8V)
NON-SELECTED WL3 (-0.2V)
NON-SELECTED WL4 (-0.2V)
NON-SELECTED Vss0 (0.2V)
NON-SELECTED Vss1 (0.2V)
SELECTED Vss2 (0V)
NON-SELECTED Vss3 (0.2V)
NON-SELECTED Vss4 (0.2V)